WHAT IS CLAIMED:

1. An image data acquisition system, comprising:

a host computer having at least one host processor executing operations with an operating system and a host memory storing data; and

a detector framing node being programmable to receive image data from a selected flat panel detector of a plurality of different flat panel detectors, and communicating the received image data to the host memory independent of the operating system.

2. The image data acquisition system according to claim 1, wherein the host computer runs a non-real time operating system, and said detector framing node continues to receive and store the image data from the selected flat panel detector during a lapse in communication with the host memory.

3. The image data acquisition system according to claim 2, wherein the received image data is radioscopic image data and the selected flat panel detector includes an amorphous silicon photo-diode array outputting the radioscopic image data in response to detection of a radiographic image.

4. The image data acquisition system according to claim 2, wherein the non-real time operating system is a task based operating system.

5. The image data acquisition system according to claim 1,

said detector framing node communicating the received image data with the host memory over a computer communication bus at a first clock frequency and receiving the image data from the selected flat panel detector over an image detection bus at a second clock frequency different from the first clock frequency.

6. The image data acquisition system according to claim 5, said detector framing node communicating with the host memory over the computer

communication bus in parallel at the first clock frequency and receiving the image data from the selected flat panel detector in serial at the second clock frequency.

7. The image data acquisition system according to claim 6, wherein the first clock frequency clocks parallel data of at least 33 MHz, and the second clock frequency clocks serial data of at least 1 GHz.

8. The image data acquisition system according to claim 5, wherein the first clock frequency is at least 33 MHz and the second clock frequency is at least 1 GHz.

9. The image data acquisition system according to claim 5, wherein the computer communication bus is a PCI bus and said detector framing node communicates with the host memory over the PCI bus in parallel.

10. The image data acquisition system according to claim 9 wherein the image detection bus is an optical fiber data link and said detector framing node receives the image data from the selected flat panel detector over the optical fiber data link in serial.

11. The image data acquisition system according to claim 1, wherein the received image data is radioscopic image data and the selected flat panel detector includes an amorphous silicon photo-diode array outputting the received radioscopic image data in response to receipt of a radiographic image.

12. The image data acquisition system according to claim 1, wherein the operating system is a task based operating system, and said detector framing node continues to receive the image data from the selected flat panel detector during a lapse in communicating the received image data from said detector framing node to the host memory.

13. The image data acquisition system according to claim 12, wherein the task based operating system is a non-real time operating system.

14. The image data acquisition system according to claim 1,

said detector framing node having a PCI interface communicating the received image data to the host memory over the computer communication bus at a first clock frequency, a fiber optic interface receiving the image data from the selected flat panel detector at a second clock frequency, and a local bus operating at a third clock frequency and communicating the received image data between the fiber optic interface and the PCI interface, the third clock frequency being greater than or equal to the first clock frequency.

15. The image data acquisition system according to claim 14,

wherein said detector framing node has a real time bus interface communicating instructions to a radiation generation system over a real time bus for triggering generation of radiation, and the image data is generated by the selected flat panel detector in response to the generated radiation.

16. The image data acquisition system according to claim 14, wherein the computer communication bus is a PCI bus, the PCI interface communicates the received image data from the local bus to the PCI bus, and the fiber optic interface receives the image data from the selected flat panel detector over an optical fiber data link.

17. The image data acquisition system according to claim 16, wherein the fiber optic interface is a serial interface receiving serial image data from the optical fiber data link, the fiber optic interface converts the serial image data into parallel image data for communication over the local bus, and the PCI interface receives the parallel image data from the local bus and communicates the parallel image data over the PCI bus at a PCI bus frequency in accordance with a PCI bus arbitration protocol.

18. The image data acquisition system according to claim 17, wherein the local bus frequency is greater than or equal to 33 MHz, such that parallel image data is communicated over the PCI bus at a rate of at least 60 MBytes/sec.

19. The image data acquisition system according to claim 14, wherein the PCI bus communicates instructions from the at least one host processor over the PCI bus to said detector framing node.

20. The image data acquisition system according to claim 14,

said detector framing node having a real time bus interface communicating instructions to a radiation generation system over a real time bus, such that the received image data is generated by the selected flat panel detector in response to the instructions communicated over the real time bus.

21. The image data acquisition system according to claim 1, said detector framing node further comprising

a fiber optic interface to receive the image data serially over an optical fiber data link and to convert the received serial image data into parallel image data, and

a PCI interface to receive the parallel image data from the fiber optic interface and communicate the parallel image data over a PCI bus at a PCI bus frequency to the host memory.

22. The image data acquisition system according to claim 1, said detector framing node selectably receiving the image data from: a cardiac/surgical digital x-ray panel having at least 1024 columns x 1024 rows of image data; a radiography digital x-ray panel having at least 2048 columns x 2048 rows of image data; or a mammography digital x-ray panel having at least 1920 columns x 2304 rows of image data.

23. The image data acquisition system according to claim 1, said detector framing node selectably receiving continuous fluoroscopy image data from: a first flat panel detector having at least 1024 columns x 1024 rows of image data; or a second flat panel detector having at least 2048 columns x 2048 rows of image data.

24. The image data acquisition system according to claim 1, said detector framing node selectably receiving continuous fluoroscopy image data from: a first flat panel detector having at least 1024 columns x 1024 rows of image data; or non-continuous fluorography image data from a first flat panel detector having at least 1024 columns x 1024 rows of image data.

25. The image data acquisition system according to claim 1, said detector framing node receiving the image data from: a single panel x-ray detection panel, such that rows of data are sequentially read out and transferred to said detector framing node, or a split panel x-ray detection panel, such that pairs of rows of data are simultaneously read out before transfer to said detector framing node.

26. The image data acquisition system according to claim 1,

said detector framing node comprising:

a PCI interface communicating the received image data to the host memory over a computer communication bus at a first clock frequency,

a fiber optic interface receiving the image data from the selected flat panel detector at a second clock frequency,

a local bus communicating the received image data between the fiber optic interface and the PCI interface, and operating at a third clock frequency greater than the first clock frequency, and

a real time bus interface communicating instructions to a radiation generation system over a real time bus, such that the image data is generated

by the selected flat panel detector in response to the instructions communicated over the real time bus to the radiation generation system,

wherein the image data is radioscopic image data.

27. The image data acquisition system according to claim 26, wherein the fiber optic interface receives serial image data and the PCI interface communicates the received image data to the at least one host processor in parallel.

28. A detector framing node, comprising:

a computer communication interface to communicate image data with a host memory of a host computer over a computer communication bus independently from control of a host processor of the host computer; and

a control unit to receive a plurality of event instructions from the host computer through said computer communication interface, the event instructions selectively controlling events in the detector framing node, a radiation generation system, or an image detection system, and said control unit executing the event instructions in real time at predetermined timing intervals.

29. The detector framing node according to claim 28, said control unit comprising:

an event queue storing the plurality of event instructions as an event instruction sequence and an acquisition control unit,

wherein the event instruction sequence is communicated to the event queue from the host computer by way of the acquisition control unit before transmission to the radiation generation system, and

wherein the event instruction sequence controls initiation, timing, and stopping of radiation generation by the radiation generation system, and the event

instruction sequence controls acquisition of the image data from the image detection system.

30. The detector framing node according to claim 29, further comprising:

a frame buffer memory unit storing the image data output from the image detection system before transmission to the host memory,

wherein said control unit receives information associated with the image data from the image detection system and transmits the associated information to the host memory as response log packets.

31. The detector framing node according to claim 29, the control unit further comprising:

a fiber optic interface communicating with the image detection system through an optical fiber data link, said fiber optic interface receiving information associated with the image data from the image detection system into a fiber optic receive unit and transmitting received event instructions to the image detection system from a fiber optic transmit unit.

32. The detector framing node according to claim 28, further comprising:

a real time bus interface receiving event instructions from the event queue for transmission to the radiation generation system, said real time bus interface notifying the control unit when the radiation generation system forces a state on the real time bus.

33. The detector framing node according to claim 28, wherein the computer communication bus is a PCI bus, the computer communication interface is a PCI interface, and the detector framing node receives the image data from an image detection system independently from storage of the received image data into the host

memory such that the detector framing node continues to receive the image data during a time period when communication over the PCI bus is not available.

34. The detector framing node according to claim 33, wherein the detector framing node communicates with the host memory over the PCI bus at a first clock frequency and receives the image data from the image detection system at a second clock frequency different from the first clock frequency.

35. The detector framing node according to claim 34, wherein the detector framing node communicates with the host memory over the PCI bus in parallel at the first clock frequency and receives the real time image data from the image detection system in serial at the second clock frequency.

36. The detector framing node according to claim 34, wherein the first clock frequency is a PCI clock frequency of at least 33 MHz, and the second clock frequency is a fiber optic transmission clock frequency of at least 1 GHz.

37. The detector framing node according to claim 33, wherein the detector framing node communicates with the host memory over the PCI bus in parallel and receives the image data from the image detection system in serial.

38. The detector framing node according to claim 33, wherein the detector framing node selectably receives the image data from: a first flat panel detector outputting at least 1024 columns x 1024 rows of data; a second flat panel detector outputting at least 2048 columns x 2048 rows of data; or a third flat panel detector outputting at least 1920 columns x 2304 rows of data.

39. The detector framing node according to claim 33, wherein the detector framing node selectably receives the image data continuously as fluoroscopy image data from a flat panel detector outputting at least 1024 columns x 1024 rows of data, or from a flat panel detector outputting at least 2048 columns x 2048 rows of data.

40. The detector framing node according to claim 33, wherein the detector framing node selectably receives the image data as real time fluoroscopy image data, or as real time fluorography image data.

41. The detector framing node according to claim 28, wherein the image data is radioscopic image data and the image detection system includes an amorphous silicon photo-diode array outputting the radioscopic image data in response to detection of a radiographic image.

42. The detector framing node according to claim 28, wherein the computer communication interface is a PCI interface and the computer communication bus is a PCI bus such that the received image data is communicated with the host memory over the PCI bus at a first clock frequency, the detector framing node further comprising:

a fiber optic interface receiving the image data from a flat panel detector at a second clock frequency; and

a local bus, operating at a third clock frequency greater than the first clock frequency, and communicating the image data between the fiber optic interface and the PCI interface.

43. The detector framing node according to claim 42, further comprising:

a real time bus interface communicating the event instructions to the radiation generation system over a real time bus,

wherein the image data is output from the flat panel detector as radioscopic image data.

44. An image data acquisition system, comprising:

a host computer having at least one host processor executing operations with an operating system and a host memory storing data; and

a detector framing node being programmable to send commands to an image detection system and receive image data from the image detection system, and communicating the received image data to the host memory independent of the operating system.

45. An image data acquisition system, comprising:

a host computer having at least one host processor executing operations with an operating system and a host memory storing data; and

a detector framing node being programmable to receive image data from an image detection system and communicate the received image data to the host memory independent of the operating system.